REMARKS

By this amendment, claims 1-10 are amended. Reconsideration in view of the above amendments and the following remarks is respectfully requested.

Applicants would like to thank the Examiner for the indication that claims 6 and 10 contain allowable subject matter. Applicants have amended claims 6 and 10 placing them in independent form and respectfully submit claims 6 and 10 should be allowed.

Upon review of this Preliminary Amendment, Applicants respectfully request the Examiner to contact Applicants' undersigned representative to schedule a personal interview on this Application.

The Office Action rejects claims 1 and 3-5 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,218,256 to Agarwal (hereinafter "Agarwal"). This rejection is respectfully traversed.

Amended claims 1, 2, 3 and 7 relate to a gate electrode structure including a silicon-containing film containing silicon as a principle constituent, a barrier metal layer formed on the silicon-containing film and a metal film with a high melting point formed on the barrier metal layer, and a method for fabricating the gate electrode structure.

Conventionally, if a barrier filmed is composed of titanium nitride (TiN), nitrogen in the barrier film reacts with the silicon in the polysilicon film to form a reaction layer composed of a silicon nitride (SiN) film at the interface, and the interface resistance increases. To help compensate for this conventional problem, an aspect of the invention relates to lowering the interface resistance between the silicon-containing film and the metal film which has a high melting point and is included in the gate electrode structure.

In accordance with claims 1 and 3, the barrier metal layer of the titanium nitride rich in titanium as compared with the stoichiometric ratio is formed between the silicon-containing film, which is formed on the gate insulating film, and the metal film having a

high melting point. Therefore, the amount of nitrogen included in the barrier metal layer is small.

Accordingly, since the barrier metal layer includes a small amount of nitrogen to be reacted with the silicon of the silicon-containing film through a high temperature annealing of the gate electrode structure, a reaction layer of a compound principally including silicon and nitrogen is never formed or, if formed, only in a small thickness between the barrier metal layer and the silicon-containing film. As a result, even when the gate electrode structure is subjected to high temperature annealing, the interface resistance between the silicon-containing film and the barrier metal layer can be prevented from increasing and therefore, the interface resistance between the silicon-containing film and the metal film which has a high melting point can be prevented from increasing.

In accordance with claims 2 and 7, since the first barrier metal layer of the titanium nitride rich in titanium as compared with the stoichiometric ratio is formed on the silicon-containing film, which is formed on the gate insulating film, the amount of nitrogen reacting with the silicon of the silicon-containing film through high temperature annealing of the gate electrode structure is small. Therefore, a reaction layer of a compound principally including silicon and nitrogen is never formed or is formed in merely a small thickness between the first barrier metal layer and the silicon-containing film. Accordingly, even when the gate electrode structure is subjected to high temperature annealing, the interface resistance between the silicon-containing film and the first barrier metal layer can be prevented from increasing and therefore the interface resistances between the silicon-containing film and the metal film that has a high melting point can be prevented from increasing.

Furthermore, since the first barrier metal layer and the second barrier metal layer, in which the nitrogen composite is higher then the stoichiometric ratio, are disposed between the silicon-containing film and the metal film with a high melting point, a

dopant introduced into the silicon-containing film is prevented from moving by the first barrier metal layer and the second barrier metal layer and hence is prevented from diffusing into the metal film with a high melting point. Also, a silicide layer of the metal having a high melting point can be avoided from being formed through a reaction between silicon of the silicon-containing film and the metal having a high melting point of the metal film.

In contrast, Agarwal is directed toward a capacitor for DRAM and its barrier layer which is different from amended claims 1 and 3 which are related to the structure and forming method of the gate electrode. According to Agarwal, a pocket (46) is formed in a substrate (10), and a lower electrode (12) lines the walls of the pocket (46) and is fabricated with HSG poly-silicon that provides a textured surface (48). Then, a dielectric (14) composed of Ta_2O_5 is layered conformable over the textured surface (48) of the lower electrode (12). After forming a barrier metal layer (16), which functions as an undercoat layer of an upper electrode (16) composed of TiN, over the dielectric (14), annealing is performed in an oxygen ambient to form the barrier metal layer (16) in an oxygen saturated state. Thereafter, an upper electrode (18) composed of a metal film with a high melting point is formed on the barrier metal layer (16).

Therefore, Applicants respectfully submit that the dielectric film (Ta_2O_5) and the barrier metal layer (TiN) are disposed between the poly-silicon film and the melting film having a high melting point. Moreover, the barrier metal layer that is rich in oxygen is formed by oxygen-annealing.

In accordance with claims 1 and 3, only the barrier metal layer that is rich in Ti and composed of TiN is formed between the silicon-containing film and the metal film having a high melting point, and a dielectric film such as that of Agarwal is not required. Furthermore, the barrier metal layer of the present invention is a TiN layer that is rich in Ti while the TiN layer of Agarwal is a TiN layer that is rich in oxygen.

In other words, in Agarwal, the dielectric film is formed between the silicon film and the barrier metal film, while in the amended claims 1 and 3, the barrier metal layer is formed directly on the silicon film. Moreover, the barrier film in Agarwal is a TiN layer rich in oxygen, while the barrier layer in the amended claims 1 and 3 is TiN layer rich in Ti.

Therefore, the structure and the effect of the gate electrode of the present invention are completely different from those of the capacitor of Agarwal.

At least based on these reasons, Applicants respectfully submit that Agarwal fails to teach, suggests or disclose each and every feature as recited in the claims 1 and 3-5. Accordingly, Agarwal fails to anticipate these claims. Withdrawal of the rejection of claims 1 and 3-5 under 35 U.S.C. §102(b) is respectfully requested.

The Office Action rejects claims 2 and 7-9 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,973,408 to Nagasaka et al. (hereinafter "Nagasaka") and further in view of U.S. Patent No. 5,561,326 to Ito et al. (hereinafter "Ito"). This rejection is respectfully traversed.

Nagasaka is directed toward a barrier layer for a contact electrode which Applicants respectfully submit is completely different then claims 2 and 7. According to Nagasaka, a second TiN film (261B) (number Ti atom arrange from 50%-59%) is formed on a contact area (42) of a Si device, a first TiN film (261A) that is rich in Ti and composed of a TiN (number Ti atom range form 62%-75%) is formed on the second TiN film (261B), and electrode wiring (151) is formed on the first TiN film (261A).

Therefore, Applicants respectfully submit that the barrier metal layer (261) is a two-layer structure. The upper-first barrier metal layer connected to the electrode wiring is a TiN layer rich in Ti, and the lower-second barrier metal layer connected to the Si is a TiN layer having almost the same stoichiometric ratio.

However, in accordance with the features of the claims, the lower-first barrier metal layer connected to the silicon-containing film is a TiN layer rich in Ti, and the upper-second barrier metal layer connected to the metal film having a high melting point has a nitrogen composition higher than the stoichiometric ratio.

Therefore, Applicants respectfully submit that the film composition of the barrier metal layer as claimed is different from that of Nagasaka such that the top and bottom layers are inversely provided.

Ito is directed toward a barrier layer for contact wiring which again Applicants respectfully submit is different than claims 2 and 7.

Specifically, in Ito, a Ti layer (185) is formed within a contact hole (183) provided in a Si substrate (180). Then, a second TiN_x layer (187) ($x = 0\text{-}1$), which nitrogen content progressively increases with respect to the Ti content, is formed on the Ti layer (185). Thereafter, a first TiN layer (186) is formed on the second TiN_x layer (187) and wiring conduct layer (182) is formed on the first TiN layer (186).

Therefore, Applicants respectfully submit that the barrier metal layer (184) is a three-layered structure, and the second TiN_x layer (the middle layer) is a TiN layer (for example, Ti_2N) rich in Ti. However, Ito at least fails to teach, suggest or disclose a TiN layer having high concentration of nitride as asserted by the Office. In other words, Ito fails to teach, suggest or disclose that the barrier layer has a nitrogen composition higher that the stoichiometric ratio.

Thus, Applicants respectfully submit that the film composition of the barrier metal layer and that of Ito are completely different.

Thus, Applicants respectfully submit that both Nagasaka and Ito fail to teach, suggest or disclose the structure and forming method of the gate electrode as claimed. Futhermore, the barrier metal layer of the present invention is completely different from

that of Nagasaka and Ito. Accordingly, Applicants respectfully submit that the cited references, either alone or in combination, fail to teach, suggest or disclose each and every aspect of the claims. Therefore, the references fail to render obvious claims 2 and 7-9. Withdrawal of the rejection claims these claims under 35 U.S.C. §103(a) is respectfully requested.

Applicants respectfully submit that the application is in condition for allowance. Favorable reconsideration and prompt allowance are respectfully requested.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner encouraged to contact Applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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Marked-up Version of the Claims

1. (Amended) [An] A gate electrode structure comprising:

a silicon-containing film formed on a gate insulating film and containing silicon as a principal constituent;

a barrier metal layer of titanium nitride rich in titanium as compared with a stoichiometric ration formed on said silicon-containing film; and

a metal film with a high melting point formed on said barrier metal layer.

2. (Amended) [An] A gate electrode structure comprising:

a silicon-containing film formed on a gate insulating film and containing silicon as a principal constituent;

a first barrier metal layer of titanium nitride rich in titanium as compared with stoichiometric ratio formed on said silicon-containing film;

a second barrier metal film of titanium nitride including nitrogen in a ration not less than a stoichiometric ration formed on said first barrier metal layer; and

a metal film with a high melting point formed on said second barrier metal layer.

3. (Amended) A method for fabricating [an] a gate electrode structure comprising the steps of:

forming, on a gate insulating film, a silicon-containing film containing silicon as a principal constituent;

forming, on said silicon-containing film, a barrier metal layer of titanium nitride rich in titanium as compared with a stoichiometric ratio;

forming a metal film with a high melting point on said barrier metal layer, whereby forming a multi-layer film including said silicon-containing film, said barrier metal layer and said metal film with a high melting point; and

patterning said multi-layer film into an electrode structure.

4. (Amended) The method for fabricating [an] a gate electrode structure of Claim 3,

wherein step of forming said barrier metal layer includes a sub-step of using a target of titanium nitride rich in titanium as compared with a stoichiometric ratio and causing discharge in an inert gas including substantially no nitrogen, whereby depositing, on said silicon-containing film, the titanium nitride rich in titanium as compared with the stoichiometric ration sputtered out from said target.

5. (Amended) The method for fabricating [an] a gate electrode structure of Claim 3,

wherein step of forming said barrier metal layer includes a sub-step of using a target of titanium including substantially no nitrogen and causing discharge in a mixed gas of a nitrogen gas and an inert gas with a partial pressure ration of the nitrogen gas lower than a nitriding point of said target, whereby depositing, on said silicon-containing film, titanium nitride rich in titanium as compared with a stoichiometric ration formed through a reaction between titanium sputtered out from said target and nitrogen ions included in said mixed gas.

6. (Amended) A method for fabricating a gate electrode structure comprising the steps of:

forming a silicon-containing film containing silicon as a principal constituent;

forming, on said silicon-containing film, a barrier metal layer of titanium nitride rich in titanium as compared with a stoichiometric ratio;

forming a metal film with a high melting point on said barrier metal layer, whereby forming a multi-layer film including said silicon-containing film, said barrier metal layer and said metal film with a high melting point; and

patterning said multi-layer film into an electrode structure,

[The method for fabricating an electrode structure of claim 3,]

wherein no titanium silicide layer is formed on said silicon-containing film

through annealing carried out on said electrode structure at a temperature of 600 or more.

7. (Amended) A method for fabricating [an] a gate electrode structure comprising the steps of:

forming, on a gate insulating film, a silicon-containing film containing silicon as a principal constituent;

forming, on said silicon-containing film, a first barrier metal layer of titanium nitride rich in titanium as compared with a stoichiometric ration;

forming, on said first barrier metal layer, a second barrier metal layer of titanium nitride including nitrogen in a ration not less than a stoichiometric ration;

forming a metal film with a high melting point on said second barrier metal layer, whereby forming a multi-layer film including said silicon-containing film, said first barrier metal layer, said second barrier metal layer and said metal film with a high melting point; and

patterning said multi-layer film into an electrode structure.

8. (Amended) The method for fabricating [an] a gate electrode structure of Claim 7,

wherein the step of forming said first barrier metal layer included a sub-step of using a target of titanium nitride rich in titanium as compared with a stoichiometric ratio and causing discharge in an inert gas included in an inert gas including substantially no nitrogen, whereby depositing, on said silicon-containing film, the titanium nitride rich in titanium as compared with the stoichiometric ration sputtered out from said target, and

the step of forming said second barrier metal layer includes a sub-step of using said target and causing discharge in a mixed gas of a nitrogen gas and an inert gas with a partial pressure ration of the nitrogen gas not less than a nitriding point of said target, whereby forming, on said target, a titanium nitride film rich in titanium as compared with the stoichiometric ration and depositing, on said first barrier metal layer, the titanium nitride rich in titanium as compared with the stoichiometric ratio sputtered out from said

titanium nitride film formed on said target.

9. (Amended) The method for fabricating [an] <u>a gate</u> electrode structure of Claim 7,

wherein the step of forming said first barrier metal layer included a sub-step of using a target including substantially no nitrogen and causing discharge in a mixed gas of a nitrogen gas and an inert gas with a partial pressure ratio of the nitrogen gas lower than a nitriding point of said target, whereby depositing, on said silicon-containing film, titanium nitride rich in titanium as compared with a stoichiometric ratio formed through a reaction between titanium sputtered out from said target and nitrogen ions included in said mixed gas, and

the step of forming said second barrier metal layer includes a sub-step of using said target and causing discharge in a mixed gas of a nitrogen gas and an inert gas with a partial pressure ration of the nitrogen gas not less than the nitriding point of said target, whereby forming, on said target, a titanium nitride film rich in titanium as compared with a stoichiometric ration and depositing, on said first barrier metal layer, the titanium nitride rich in titanium as compared with the stoichiometric ration sputtered out from said titanium nitride film formed on said target.

10. (Amended) <u>A method for fabricating a gate electrode structure comprising the steps of:</u>

<u>forming a silicon-containing film containing silicon as a principal constituent;</u>

<u>forming, on said silicon-containing film, a first barrier metal layer of titanium nitride rich in titanium as compared with a stoichiometric ration;</u>

<u>forming, on said first barrier metal layer, a second barrier metal layer of titanium nitride including nitrogen in a ration not less than a stoichiometric ration;</u>

<u>forming a metal film with a high melting point on said second barrier metal layer, whereby forming a multi-layer film including said silicon-containing film, said first barrier metal layer, said second barrier metal layer and said metal film with a high</u>

melting point; and

patterning said multi-layer film into an electrode structure,

[The method for fabricating an electrode structure of claim 7,]

wherein no titanium silicide layer is formed on said silicon-containing film through annealing carried out on said electrode structure at a temperature of 600 or more.